Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS

1. (Currently Amended) A microprocessor comprising:

a unit to insert a first micro-operation into an instruction stream, the first micro-operation to defer renaming of a plurality of registers defined by predicated instructions, upon which a common instruction depends;

a plurality of register renaming units to rename at least one register corresponding to the predicated instructions ~~after the common instruction is executed~~, wherein the common instruction is to use data from a plurality of destination registers corresponding to the first micro-operation;

an augmented register alias table.

2. (Currently Amended) The microprocessor of Claim 1, wherein [[the]] a register renaming unit renames each one of a plurality of source registers of the pipeline instruction and renames a destination register to a new physical register.

3. (Original) The microprocessor of Claim 2, wherein the augmented register alias table includes a plurality of lines, and wherein each one of the plurality of lines includes a plurality of renamed destination registers.

4. (Original) The microprocessor of Claim 3, wherein each one of a plurality of select-μops has a plurality of source operands wherein each one of the plurality of source operands corresponds to a physical register identifier.

5. (Original) The microprocessor of Claim 4, wherein the plurality of source operands comprises a first source operand and a plurality of secondary source operands.

6. (Original) The microprocessor of Claim 5, wherein the first source operand includes a default physical register identifier, wherein the default physical register is always valid and available.

7. (Original) The microprocessor of Claim 5, wherein each one of the plurality of secondary source operands includes a plurality of status bits and a physical register identifier.

8. (Currently Amended) The microprocessor of Claim 7, wherein ~~each one of~~ the plurality of status bits has a ready bit and a committed bit.

9. (Currently Amended) A method of processing predicated instructions comprising:

receiving a plurality of predicated instructions assigned to a common defined destination register and wherein at least one of the plurality of predicated instructions is out of order in [[an]] a dynamic pipeline;

renaming the destination register for each of the plurality of predicated instructions;

assigning the corresponding renamed destination register for each one of the plurality of predicated instructions with a corresponding predicate register to corresponding ones of [[the]] a plurality of source operands of a select-μop;

determining a valid predicate in the source operands of the select-μop;

selecting [[the]] a register corresponding to the select-μop that corresponds to the valid predicate;

transferring the data in the selected register to [[the]] a destination register; and

executing a consumer instruction ~~before renaming the destination register of each of the plurality of predicated instructions~~, wherein the consumer instruction uses the data from the destination register of the corresponding select-μop.

10. (Currently Amended) The method of Claim 9, wherein [[the]] each one of [[the]] a plurality of select-μops has a plurality of source operands wherein each one of the plurality of source operands corresponds to a physical register identifier.

11. (Original) The method of Claim 10, wherein the plurality of source operands comprises a first source operand and a plurality of secondary source operands.

12. (Original) The method of Claim 11, wherein the first source operand includes a default physical register identifier, wherein the default physical register is always valid and available.

13. (Original) The method of Claim 11, wherein each one of the plurality of secondary source operands includes a plurality of status bits and a physical register identifier.

14. (Currently Amended) A computer system comprising:

a processor, wherein the processor includes:

a unit to insert a first micro-operation into an instruction stream, the first micro-operation to defer renaming of a plurality of registers defined by different predicated instructions, upon which a dependent instruction depends;

a plurality of execution units to execute the dependent instruction;

a reorder buffer;

a plurality of register renaming units to rename at least one register corresponding to a predicated instruction ~~after the dependent instruction is executed~~, wherein the dependent instruction is to use data from a plurality of destination registers corresponding to the first micro-operation;

a plurality of reservation stations wherein [[the]] a register renaming unit, the reorder buffer, the plurality of execution units and the plurality of reservation stations are coupled to at least one of a plurality of dynamic pipeline stages; and

an augmented register alias table;

a system bus;

a computer memory system;

an input/output device;

wherein the system bus is coupled to the processor, the computer memory system and the input/output device.

15. (Original) The computer of Claim 14 wherein, the augmented register alias table includes a plurality of lines, and wherein each one of the plurality of lines includes a plurality of renamed destination registers.

16. (Currently Amended) The computer of Claim 15 wherein, the register renaming unit renames each one of [[the]] a plurality of source registers of [[the]] a pipeline instruction and renames the destination register to a new physical register.